WHAT IS CLAIMED IS:

1. A loop apparatus, comprising:

a plurality of gain stages connected in series to amplify a signal having a voltage, wherein each gain stage increases the voltage of the signal, and includes an input port that receives the signal and an output port that transmits the resulting amplified signal; and

a plurality of feedback loops that cancel an undesired offset of the resulting amplified signal, wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset of its corresponding gain stage.

2. The loop apparatus of claim 1, wherein the undesired offset is a direct current offset voltage, and each feedback loop includes a direct current offset canceling unit for rejecting the direct current offset voltage accumulated by its corresponding gain stage.

3. The loop apparatus of claim 2, wherein each direct current offset canceling unit includes a high-pass filter that filters the direct current offset voltage.

4. The loop apparatus of claim 1, wherein each gain stage includes a variable gain amplifier.

5. The loop apparatus of claim 1, wherein the plurality of gain stages and feedback loops are mounted on a chip, and each feedback loop includes a capacitor mounted on the chip.

6. The loop apparatus of claim 1, wherein the signal is an analog radio frequency signal.

7. A method for controlling a gain of a signal, comprising:

amplifying the voltage of a signal by propagating the signal through a plurality of gain stages connected in series, wherein each gain stage increases the voltage of the signal, and includes an input port receiving the signal and an output port transmitting the resulting amplified signal; and

canceling an undesired offset of the resulting amplified signal with a plurality of feedback loops, wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset of its corresponding gain stage.

8. A direct conversion receiver, comprising:

an amplification unit that receives and amplifies a signal, wherein the amplification unit includes

a plurality of gain stages connected in series to amplify the signal having a voltage, wherein each gain stage increases the voltage of the signal, and includes an input port that receives the signal and an output port that transmits the resulting amplified signal, and

a plurality of feedback loops that cancel an undesired offset of the resulting amplified signal, wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset of its corresponding gain stage; and

a mixer that demodulates the amplified signal by mixing the amplified signal with a local oscillation signal to form a demodulated baseband signal.

9. The direct conversion receiver of claim 8, further comprising an analog-to-digital converter that converts the demodulated baseband signal to a digital data stream.

10. The direct conversion receiver of claim 9, further comprising a channel selection filter that removes an out-of-band signal from the demodulated baseband signal.

11. The direct conversion receiver of claim 8, wherein the undesired offset is a direct current offset voltage, and each feedback loop includes a direct current offset canceling unit for rejecting the direct current offset voltage accumulated by its corresponding gain stage.

12. The direct conversion receiver of claim 11, wherein each direct current offset canceling unit includes a high-pass filter that filters the direct current offset voltage.

13. The direct conversion receiver of claim 8, wherein each gain stage includes a variable gain amplifier.

14. The direct conversion receiver of claim 8, wherein the plurality of gain stages and feedback loops are mounted on a chip, and each feedback loop includes a capacitor mounted on the chip.

15. The direct conversion receiver of claim 8, wherein the signal is an analog radio frequency signal.

16. The direct conversion receiver of claim 8, wherein the mixer receives a plurality of clock signals to generate the local oscillator signal, wherein each of the clock signals has a frequency less than the local oscillator signal.